STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES

Claims 1-26 are pending and stand rejected. Claims 1-20 are allowable over the cited art but are rejected due to an allegedly defective declaration. Claims 21-26 are rejected based on cited art.

In response, Applicant hereby submits a revised declaration, amends claims 21 and 26 relative to the preliminary amendment, and adds new claims 27-36 directed to a memory access controller and a data transmission method. Claims 1-36 are pending upon entry of this amendment.

Support for new claims 11-36 is found in the specification of the issued patent at col. 3, line 57 through col. 6, line 17 et seq. and in Figures 1-8.

REMARKS

Applicant thanks the Examiner for the telephone conference related to the declaration conducted on August 14, 2006 and for the conference related to the prosecution history of the original patent conducted in early September.

Reissue Declaration

The Examiner asserts that the reissue declaration filed with this application is defective because "new claims have been submitted without specifically pointing out the differences from the original claims" (quoting from paragraph 1 of the Office Action). In response, Applicant submits a revised declaration.

Applicant respectfully notes that neither 37 CFR 1.175 nor MPEP §1414 requires the declaration to specifically point out differences between new and original claims. Rather, the MPEP §1414 states that "Any error in the claims must be identified by reference to the specific claim(s) and the specific claim language wherein lies the error." Applicant submits that the revised declaration meets this requirement by stating that an error is failure to claim or further claim subject matter pertaining to a memory access controller and lacking the "computer system memory" recited by claim 8. Applicant has also revised the description of the error to more closely track the language of the claims.

Applicant submits that the revised declaration meets the requirements of the CFR and MPEP. If the Examiner maintains this rejection, Applicant respectfully request that the Examiner provided a detailed explanation of the rejection to allow Applicant to fully address the Examiner's concerns.

35 U.S.C. §102(e) Rejections

Claims 21-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Kawai et al. (U.S. Patent No. 5,584,010). Applicant has amended independent claims 21 and 26 relative to the preliminary amendment to clarify the subject matter being claimed.

Claim 21 now recites a memory access controller adapted to be coupled to a computer system memory and an I/O device, comprising:

> a register for storing a data status signal generated by the I/O device after the I/O device transfers a data unit **to a system external to the computer system**.

Claim 26 now recites a similar feature. Independent claims 30 and 34 recite a data status signal generated after a data unit transfer between the computer system memory and a system external to the computer system. The claims now explicitly recite that the I/O device generates the data status signal after completion of a data transfer between the computer system and a system external to the computer system.

Kawai, in contrast, does not disclose generating a data status signal after a data unit is transferred between a computer and a system external to the computer. Kawai discloses a multi-processor system having multiple digital signal processors (DSPs). Each DSP has an internal memory, and can use direct memory access (DMA) to exchange data with the other DSPs. In addition, the multi-processor system has an external data memory that the DSPs can access via a main data bus (See FIG. 5, and col. 6, line 65 to col. 7, line 24). The Examiner asserts that Kawai's "external data memory" is the "external system" previously recited by the claims.

While Kawai refers to an "external data memory," this memory is not "external to the computer system" as recited by claims 21, 26, 30, and 34. Kawai uses the term "external" to draw a distinction between the DSPs' internal memories and the multiprocessor system's main memory. Kawai does not disclose that the DSPs can communicate with a system external to the

multiprocessor system, and therefore does not disclose a register for storing a data status signal generated after a data unit is transferred with such a system.

For the above reasons, Applicant respectfully submits that the reissue declaration complies with 37 CFR 1.175 and that the pending independent claims are not anticipated by Kawai. The rejected dependent claims incorporate the elements of their respective base claims and are not anticipated for at least the same reasons. Accordingly, Applicant respectfully requests that the Examiner allow this application. The Examiner is invited to contact the undersigned to advance prosecution of this case.

Respectfully submitted,
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Dated: September 25 ,2006

By: _____

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